

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A method for calibrating a device, the device comprising a plurality of transconductor cells, the method comprising the steps of:
  - (a) generating a test signal to the device; and
  - (b) suppressing even-order harmonics due to transistor mismatches within the plurality of transconductor cells, wherein the suppressing step (b) comprises the step of (b1) introducing an offset voltage on an amplifier in the plurality of transconductor cells that controls the drain to source voltage of the input transistors of the cells.
2. (canceled)
3. (currently amended) The method of claim 2 1, wherein the offset voltage is controlled by a DSP in order to minimize the even order harmonics upon the application of the test signal on the device.
4. (original) The method of claim 1 wherein the device comprises a second order low pass filter.

5. (original) The method of claim 1 wherein the test signal comprises a sinusoidal test signal.
6. (currently amended) A calibration system comprising a device, the device including a plurality of transconductor cells; and  
a digital signal processor (DSP), the DSP for generating a test signal to the device and for suppressing even order harmonics due to transistor mismatches within the plurality of transconductor cells, wherein the DSP introduces an offset voltage to each amplifier in a plurality of transconductor cells that control the drain to source voltage of the input transistors of the cells.
7. (canceled)
8. (original) The system of claim 6 wherein the device comprises a second order low pass filter.
9. (currently amended) The system of claim ~~7~~ 6 wherein the DSP controls the offset voltage in order to minimize the even order harmonics upon the application of the test signal on the device.
10. (original) The system of claim 6 wherein the test signal comprises a sinusoidal test signal.